

許健 老師

現職 資訊工程學系 教授級專業技術人員

學歷 University of Iowa -- 博士

教師研究成果資料明細

研究計畫

1.許健 其他單位 2008.05.1 ~2009.04.31

與世界先進積體電路股份有限公司產學合作

2.許健 其他單位 2009.05.1 ~2009.07.31

與世界先進積體電路股份有限公司產學合作

3.許健 其他單位 2010.09.1 ~2012.08.31

臺灣積體電路有限公司委託研究

4.許健 其他單位 2011.09.1 ~2013.08.31

新唐科技委託研究

SCI、SSCI、A&HCI、EI、TSSCI期刊論文

1.游信強(Hsin-Chiang You)、曹世昌(Shyh-Chang Tsaur)、許健(Gene Sheu),2009-03, (已刊登)

Semiconductor Science and Technology 18卷1期:129頁~133頁

Simulation Details for the Electrical Field Distribution and Breakdown Voltage of 0.15 μ m Thin Film SOI Power Device

2.許健(Gene Sheu)、楊紹明(Shao-Ming Yang),2009-01, (已刊登)

Semiconductor Science and Technology 18卷1期:123頁~124頁

A High Performance 80V Smart LDMOS Power Device Based on Thin SOI Technology

3.郭宇鋒(Yufeng Guo)、王至剛(Zhigong Wang)、許健(Gene Sheu),2009-07, (已刊登)

2009 International Conference on Communications, Circuits and Systems

(ICCCAS2009) 2009卷july期:611頁~613頁

Variation of Lateral Thickness techniques in SOI Lateral High Voltage Transistors

4.楊紹明(Shao-Ming Yang)、許健(Gene Sheu),2009-, (已刊登)

The Ninth International Conference on Electronic Measurement & Instruments

4卷9期:594頁~597頁

Dependence of Breakdown Voltage on Drift Length and Linear Doping Gradients in SOI RESURF LDMOS Devices

5.郭宇峰(Yufeng Guo)、(Zhigong Wang)、許健(Gene Sheu),2009-, (已刊登)

Journal of Semiconductors 30卷11期:114006-1頁~114006-4頁

A Three-dimensional Breakdown Model of SOI Lateral Power Transistors with a Circular Layout

6. 郭宇峰(Yufeng Guo)、(Zhigong Wang)、許健(Gene Sheu),2009-11, (已刊登)
Journal of Semiconductors 30卷11期:114006-1頁~114006-4頁
A Three-dimensional Breakdown Model of SOI Lateral Power Transistors with a Circular Layout
7. 許健(Gene Sheu)、楊紹明(Shao-Ming Yang),2010-02, (已刊登)
ECS Transactions 27卷1期:125頁~129頁
Combining 2D and 3D Device Simulations for Optimizing LDMOS Design
8. 許健(Gene Sheu)、楊紹明(Shao-Ming Yang),2010-03, (已刊登)
ECS Transactions 27卷1期:125頁~129頁
Combining 2D and 3D Device Simulations for Optimizing LDMOS Design
9. 郭宇峰(GUO Yu-Feng)、王志功(WANG Zhi-Gong)、許健(Gene Sheu),2010-, (已刊登)
CHINESE PHYSICS LETTERS 27卷6期:067301-1頁~067301-4頁
A High Performance Silicon-on-Insulator LDMOSTT Using Linearly Increasing Thickness Techniques
10. 許健(Gene Sheu)、楊紹明(Shao-Ming Yang),2010-07, (已刊登)
JAPANESE JOURNAL OF APPLIED PHYSICS 49卷2010期:074301-1頁~074301-8頁
An Analytical Model of Surface Electric Field Distributions in Ultrahigh-Voltage Metal-Oxide-Semiconductor Devices
11. 許健(Gene Sheu)、楊紹明(Shao-Ming Yang),2010-02, (已刊登)
ECS Transactions 27卷1期:115頁~120頁
Reduction of Kink Effect in SOI LDMOS Structure with Linear Drift Region Thickness
12. 許健(Gene Sheu)、楊紹明(Shao-Ming Yang),2010-03, (已刊登)
ECS Transactions 27卷1期:115頁~120頁
Reduction of Kink Effect in SOI LDMOS Structure with Linear Drift Region Thickness
13. 許健(Gene Sheu)、楊紹明(Shao-Ming Yang)、陳兆南,2010-02, (已刊登)
ECS Transactions 27卷1期:103頁~108頁
Comparison of High Voltage (200-300 Volts) Lateral Power MOSFETs for Power Integrated Circuits
14. 許健(Gene Sheu)、楊紹明(Shao-Ming Yang)、陳兆南,2010-03, (已刊登)
ECS Transactions 27卷1期:103頁~108頁
Comparison of High Voltage (200-300 Volts) Lateral Power MOSFETs for Power Integrated Circuits
15. 許健(Gene Sheu)、楊紹明(Shao-Ming Yang)*、張怡楓(Yi-Fong Chang)、曹世昌(Shyh-Chang Tsaur),2010-07, (已刊登)
JAPANESE JOURNAL OF APPLIED PHYSICS 卷49期:74301頁~74308頁
An Analytical Model of Surface Electric Field Distributions in Ultrahigh-Voltage Buried P-top Lateral Diffused Metal-Oxide-Semiconductor Devices
16. 楊紹明(Shao-Ming Yang)、許健(Gene Sheu)、蔡宗勳(Jung-Ruey Tsai),2010-11, (已刊登)
ICSICT-2006: 2006 8th International Conference on Solid-State and Integrated Circuit Technology, Proceedings 1卷3期:1838頁~1840頁

A 5V/200V SOI Device with a Vertically Linear Graded Drift Region

17.許健(Gene Sheu) ,2011-, (已刊登)

ECS Transactions 34卷1期:979頁~984頁

LDMOS Thermal SOA Investigation of a Novel 800V Multiple RESURF with

18.許健(Gene Sheu) ,2010-11, ()

ICSICT-2006: 2006 8th International Conference on Solid-State and Integrated Circuit Technology, Proceedings 2010卷2010期:1850頁~1852頁

A 2D Analytical Model of Bulk-silicon Triple RESURF Devices

19.許健(Gene Sheu) ,2010-11, (已刊登)

ICSICT-2006: 2006 8th International Conference on Solid-State and Integrated Circuit Technology, Proceedings 2010卷期:1850頁~1852頁

A 2D Analytical Model of Bulk-silicon Triple RESURF Devices

20.許健(Gene Sheu) 、楊紹明(Shao-Ming Yang) 、曹世昌(Shyh-Chang Tsaur) ,2009-, ()

SEMICONDUCTOR SCIENCE AND TECHNOLOGY 卷期:頁~頁

An Analytical Model for Surface Electric Field Distributions in Ultra High Voltage (800V) Buried P-top LDMOS Devices

21.許健(Gene Sheu) 、楊紹明(Shao-Ming Yang) 、曹世昌(Shyh-Chang Tsaur) ,2009-, ()

SEMICONDUCTOR SCIENCE AND TECHNOLOGY 卷期:頁~頁

Comparison of High Voltage (200-300 Volts) Devices for Power Integrated Circuits

22.楊紹明(Shao-Ming Yang) 、許健(Gene Sheu) ,2009-, ()

APPLIED PHYSICS LETTERS 卷期:頁~頁

The Reliability of 200V P-channel Silicon-On-Insulator LDMOS on High Side operation

23.許健(Gene Sheu) 、楊紹明(Shao-Ming Yang) ,2009-03, (已刊登)

ECS Transactions 18卷期:123頁~128頁

A High Performance 80V Smart LDMOS Power Device Based on Thin SOI Technology

24.許健(Gene Sheu) 、楊紹明(Shao-Ming Yang) ,2010-11, ()

IEEE Region 10 Annual International Conference, Proceedings/TENCON

卷2010期:71頁~74頁

An 800 Volts High Voltage Interconnection Level Shifter Using Floating Poly Field Plate (FPFP) Method

25.許健(Gene Sheu) 、楊紹明(Shao-Ming Yang) ,2010-11, (已刊登)

IEEE Region 10 Annual International Conference, Proceedings/TENCON

卷1期:71頁~74頁

An 800 Volts High Voltage Interconnection Level Shifter Using Floating Poly Field Plate (FPFP) Method

26.許健(Gene Sheu) 、楊紹明(Shao-Ming Yang) ,2010-11, ()

IEEE Region 10 Annual International Conference, Proceedings/TENCON

2010卷2010期:75頁~79頁

A Novel 800V Multiple RESURF LDMOS Utilizing Linear P-top Rings

27.許健(Gene Sheu) 、楊紹明(Shao-Ming Yang) ,2010-11, (已刊登)

IEEE Region 10 Annual International Conference, Proceedings/TENCON

卷1期:75頁~79頁

A Novel 800V Multiple RESURF LDMOS Utilizing Linear P-top Rings

28.許健(Gene Sheu)、楊紹明(Shao-Ming Yang),2010-10, (已刊登)
IEEE Region 10 Annual International Conference, Proceedings/TENCON
卷1期:80頁~83頁
ESD Simulation on GGNMOS for 40V BCD

29.楊紹明(Shao-Ming Yang)、許健(Gene Sheu)、蔡宗叡(Jung-Ruey Tsai),2011-08, (已刊登)
ICEMI 1卷期:85頁~88頁
Application of Multi-Lateral Double Diffused Field Ring in Ultrahigh-Voltage Device MOS Transistor Design

30.蔡宗叡(Jung-Ruey Tsai)、許健(Gene Sheu)、楊紹明(Shao-Ming Yang),2011-08, (已刊登)
ICEMI 1卷期:235頁~238頁
Analysis of Si₃N₄ passivation effect by self-consistent electro-thermal-mechanical simulation in AlGa_N/Ga_N heterostructure HEMTs

31.楊紹明(Shao-Ming Yang)、許健(Gene Sheu)、蔡宗叡(Jung-Ruey Tsai),2011-08, (已刊登)
ICEMI 1卷期:239頁~242頁
Effects of SiO₂ passivation on AlGa_N/Ga_N HEMT by self-consistent electro-thermal-mechanical simulation

32.許健(Gene Sheu)、蔡宗叡(Jung-Ruey Tsai)*、楊紹明(Shao-Ming Yang),2011-08, (已刊登)
The Ninth International Conference on Electronic Measurement & Instruments 4卷期:5頁~9頁
Improvement of Electrical Characteristics in LDMOS by the Insertion of PBL and Gate Extended Field Plate Technologies

33.許健(Gene Sheu)、蔡宗叡(Jung-Ruey Tsai)*、楊紹明(Shao-Ming Yang),2011-08, (已刊登)
ICEMI 4卷期:5頁~9頁
Improvement of Electrical Characteristics in LDMOS by the Insertion of PBL

非SCI、SSCI、A&HCI、EI、TSSCI...等具審查機制論文

1.許健(Gene Sheu)、楊紹明(Shao-Ming Yang),2011-07, (已刊登)
tencon 2010 2010卷期:978頁~990頁
ESD simulation on GGNMOS for 40V BCD

2.許健(Gene Sheu)、楊紹明(Shao-Ming Yang),2011-, (已刊登)
tencon 2010 2010卷2010期:75頁~77頁
A Novel 800V Multiple RESURF LDMOS Utilizing

3.許健(Gene Sheu)、楊紹明(Shao-Ming Yang),2011-07, (已刊登)
tencon 2010 2010卷2010期:71頁~74頁
An 800 Volts High Voltage Interconnection Level

4.許健(Gene Sheu),2011-, (已刊登)
2010 IRAST International Congress on Computer Applications and computational science 2010卷2010期:頁~頁
A 2-dimensional mesh study using sentaurus simulator

5.楊紹明(Shao-Ming Yang)、許健(Gene Sheu)、蔡宗叡(Jung-Ruey Tsai)

,2010-11, ()

ICSICT 2010 2010卷2010期:1838頁~1840頁

A 5V/200V SOI Device with a Vertically Linear Graded Drift Region

6. 楊紹明(Shao-Ming Yang)、許健(Gene Sheu)、蔡宗叡(Jung-Ruey Tsai)

,2010-11, (已刊登)

ICSICT 2010 卷期:1838頁~1840頁

A 5V/200V SOI Device with a Vertically Linear Graded Drift Region

7. 許健(Gene Sheu)、蔡宗叡(Jung-Ruey Tsai)、楊紹明(Shao-Ming Yang)

,2011-11, (已刊登)

tencon 2010 卷期:1356頁~1360頁

Self-Consistent Electro-Thermo-Mechanical Analysis of AlN Passivation Effect on AlGaIn/GaN HEMTs

8. 蔡宗叡(Jung-Ruey Tsai)、許健(Gene Sheu)、楊紹明(Shao-Ming Yang)

,2011-11, (已刊登)

tencon 2010 卷期:760頁~763頁

Development of ESD Robustness Enhancement of a Novel 800V LDMOS Multiple RESURF with Linear P-top Rings

9. 許健(Gene Sheu)、楊紹明(Shao-Ming Yang)、蔡宗叡(Jung-Ruey Tsai)

,2011-11, (已刊登)

tencon 2010 卷期:752頁~755頁

Design of Multiple RESURF LDMOS with P-top rings and STI regions in 65nm CMOS Technology

研討會論文

1. 許健(Gene Sheu)、許健(Gene Sheu) 2009.08.15~2009.08.19

Dependence of Breakdown Voltage on Drift Length and Linear Doping Gradients in SOI RESURF LDMOS Devices

2009 ICEMI

2. 郭宇鋒(Yufeng Guo)、王至剛(Zhigong Wang1)、許健(Gene Sheu)、許健(Gene Sheu) 2009.07.23~2008.07.25

VARIATION OF LATERAL THICKNESSTECHNIQUES IN SOI LATERAL HIGH VOLTAGE DEVICE

2009 International Conference on Communications, Circuits and Systems(ICCAS2009)

3. 許健(Gene Sheu)、許健(Gene Sheu) 2009.12.13~2009.12.16

Combining 2D and 3D Device Simulation for Optimizing LDMOS Design
2009 IEEE International Conference on Electronics Circuits and Systems

4. (Hsin-Chiang You)、(Yen-Ling Liu)、(Shyh-chang Tsaur)、許健(Gene Sheu)、許健(Gene Sheu) 2009.03.19~2009.03.20

Simulation Details for the Electrical Field Distribution and Breakdown Voltage of 0.15 μ m Thin Film SOI Power Device

The Electrochemical Society Transaction 2009 (©ISTC CSTIC 2009)

5. 許健(Gene Sheu)、楊紹明、許愉珊、許健(Gene Sheu)

2009.05.24~2009.05.25

A High Performance 80V Smart LDMOS Power Device Based on thin oxide technology

istc cstic 2009

6. 楊紹明(Shao-Ming Yang) 、許健(Gene Sheu) 2009.08.16~2009.08.19
Dependence of Breakdown Voltage on Drift Length and Linear Doping Gradients in SOI RESURF LDMOS Devices
The International Conference on Electronic Measurement & Instruments (ICEMI)

7. 楊紹明(Shao-Ming Yang) 2010.08.3 ~2010.08.6
Optimizing NSCR ESD Protection Device for BCD 40V Technology
第二十一屆超大型積體電路設計暨計算機輔助設計技術研討會